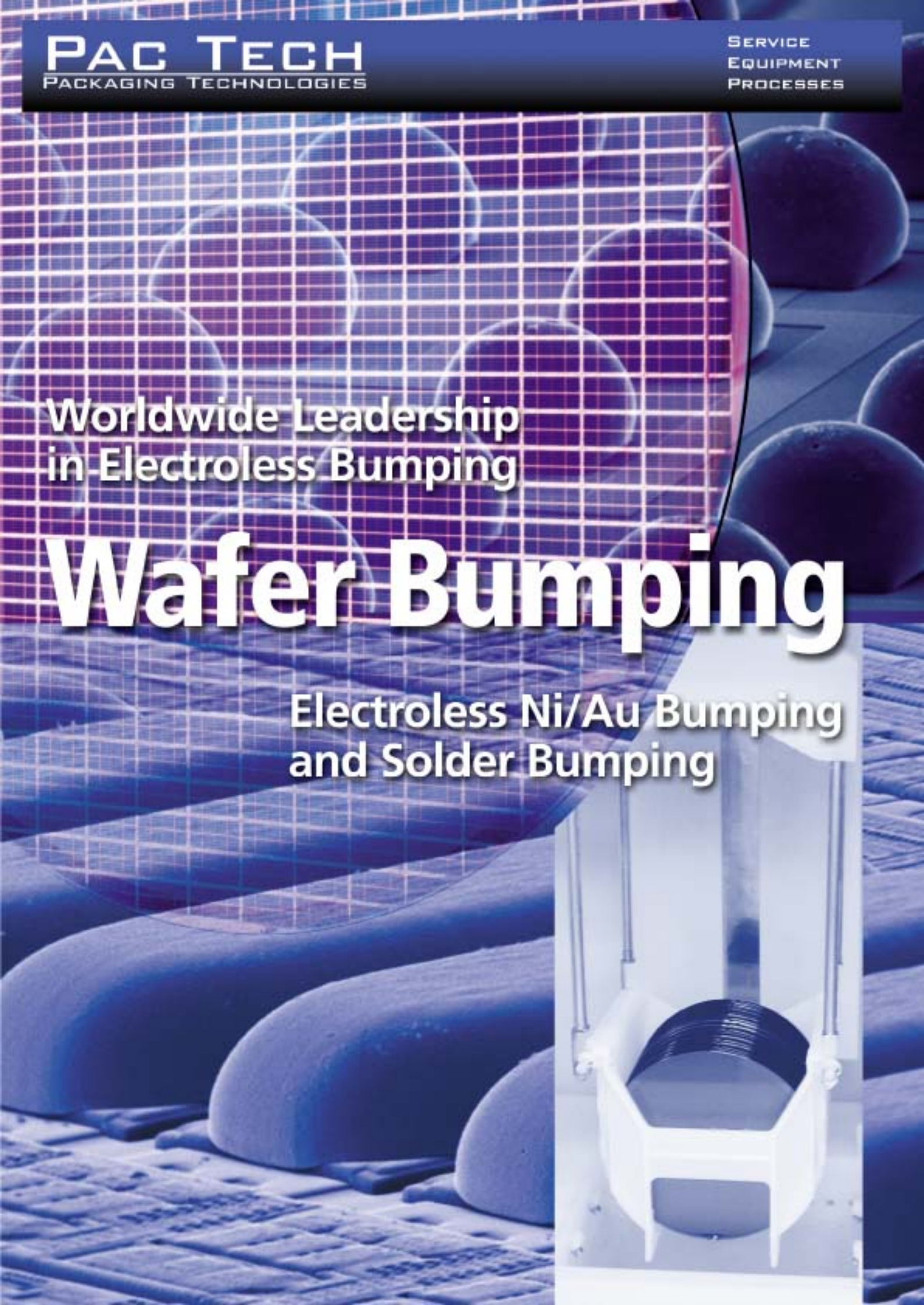


Worldwide Leadership
in Electroless Bumping

Wafer Bumping

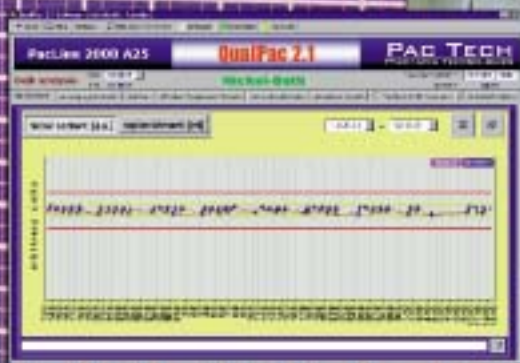
Electroless Ni/Au Bumping
and Solder Bumping



Pac Tech

About Pac Tech

Pac Tech GmbH was founded in 1995 and is the world's leading wafer bumping and packaging subcontractor based on electroless metallization. Since its inception, Pac Tech has received 20 patents for products developed in areas relating to wafer bumping, flip chip, chip-scale packaging and laser bonding technologies. Pac Tech has formed alliances with companies in the U.S., Europe and Asia for licensing, equipment sales and wafer bumping services.



Automatic wafer handling

Pac Tech's electroless bumping process

A proven and reliable state of the art technology,
DIN EN ISO 9001 superior quality management.

Special benefits: Low cost, high volume, high throughput,
high flexibility-wafer size 2" up to 12"

Applied on aluminum and copper pad metallization

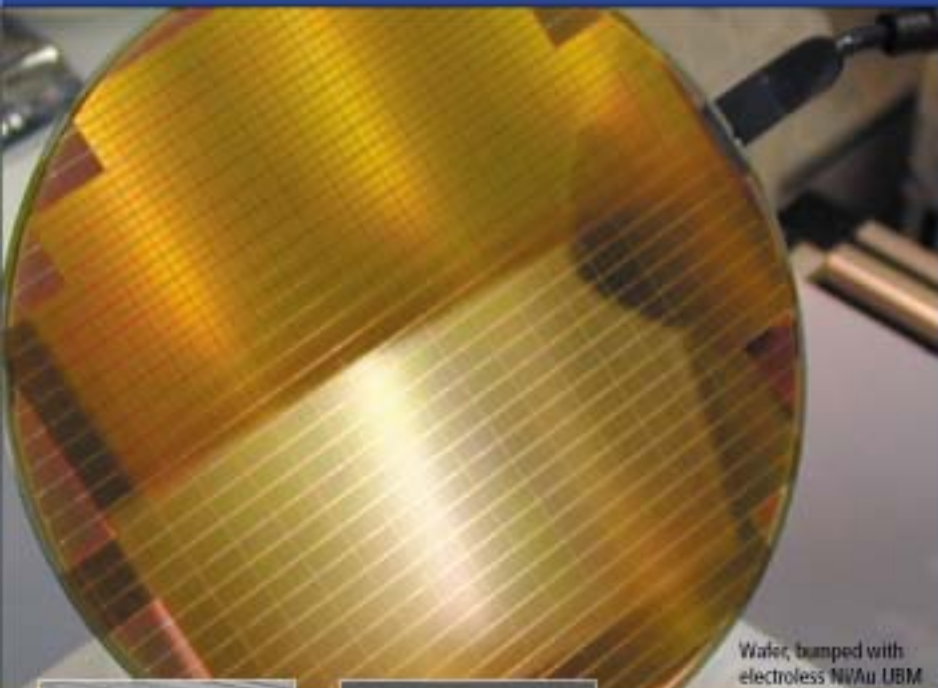
Suitable for all state of the art Flip Chip assembly methods: Soldering (eutectic & leadfree),
Anisotropic Conductive Film (ACF), Non Conductive Film (NCF), Isotropic Conductive Adhesive (ICA)

- Qualified applications:
- medical
 - automotive
 - telecommunication
 - consumer electronics
 - LCD-drivers
 - data communication
 - computer electronics
 - optoelectronics
 - smart cards/smart labels



Flip chip on Board

Worldwide Leader in Electroless Bumping



Wafer, bumped with electroless Ni/Au UBM

Electroless Ni/Au Bumping on Al and Cu pad

Pac Tech's unique low cost process allows both, an electroless Ni/Au deposition as a thin Under Bump Metallization-UBM ($5\mu\text{m}$) or alternatively a thick bump ($10\text{-}25\mu\text{m}$). This automatic wet chemical production process is using the proprietary Pac Tech Controllomat and QualPac Software.

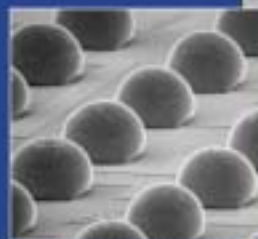
Today's applications are focused mainly on wafer pads consisting of aluminum and aluminum alloys. In the next generation electroless Ni/Au is applied on high end wafers with copper pad metallization. On copper pads, electroless Ni/Au offers a universal applicable metallization for Flip Chip and Wire Bonding.



Electroless Ni/Au for flip chip



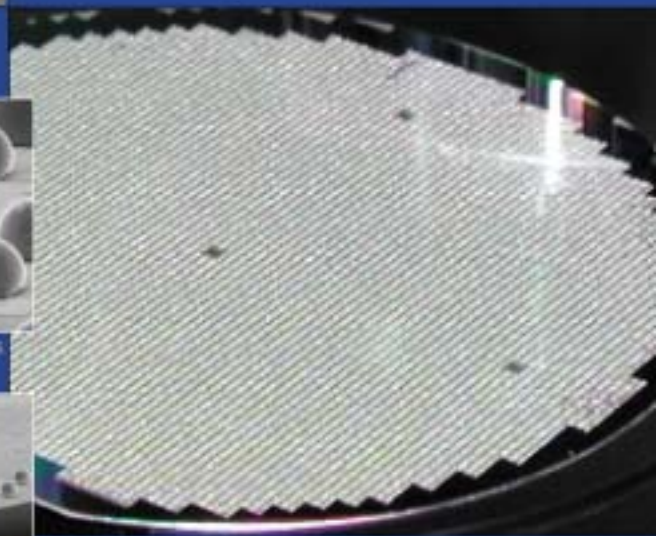
Electroless Ni/Au for wire bond



Eutectic solder bumps



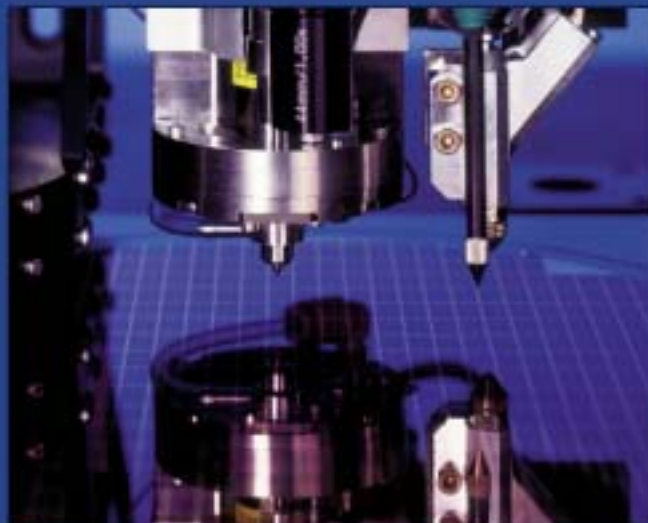
Leadfree solder bumps



Solder Bumping

For SMT-compatible Flip Chip assembly processes, Pac Tech offers a wafer level solder bumping process. The solder is deposited by ultra fine pitch wafer level stencil printing. Alternatively, Pac Tech's ball placement technology using SB² and SB²-Jet are used for special applications.

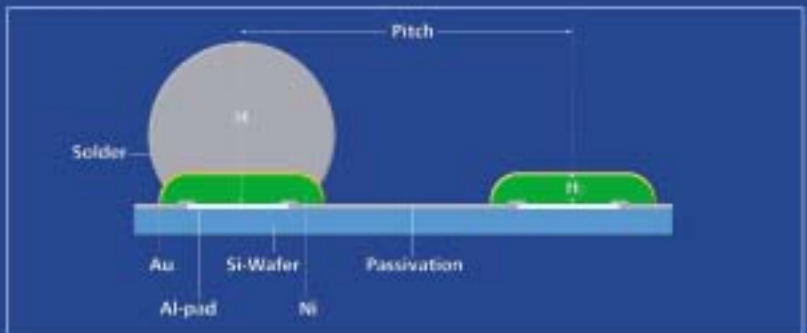
Stencil printing is a low cost high volume production process which allows a high variety of solder alloys (eutectic SnPb, lead-free SnAg, SnAgCu and others).



SB²-Jet

Fluxless Solder Bumping for Optoelectronic devices & MEMS

With the automatic, SB² (Solder Ball Bumping) System, Pac Tech offers a unique solution for optoelectronic, MEMS and sensor devices. The SB²-bondhead provides fluxless placement and local laser reflow of solder balls. It allows a high variety of solder alloys (highlead PbSn, eutectic SnPb, leadfree Sn-based alloys, AuSn 80/20). Typical solder ball diameters are in the range of $80\mu\text{m}$ up to $760\mu\text{m}$.



Technical Specifications

| Features | electroless Ni/Au Bump | eutectic SnPb | leadfree Sn95,5Ag4Cu0,5 |
|---|---|--|--|
| α -Emission | low alpha | | low alpha |
| Wafer sizes | 4", 5", 6", 8", 12" | 4", 5", 6", 8", 12" | 4", 5", 6", 8", 12" |
| Minimum wafer thickness | 150 μ m | 200 μ m | 200 μ m |
| Pad metalization | Al: AlSi, AlSiCu, AlCu others: Cu, Pd | Al: AlSi, AlSiCu, AlCu, Cu others: Cu, Pd | Al: AlSi, AlSiCu, AlCu, Cu others: Cu, Pd |
| Standard bump height | 2 – 5 μ m (UBM) 10 – 25 μ m (Adhesive-bump) | 80 – 300 μ m* | 100 μ m |
| Bump height uniformity | +/- 5% (wafer) | +/- 10% (wafer) | +/- 15% (wafer) |
| Minimum pitch | 50 μ m | 150 μ m | 150 μ m |
| Minimum pad size | 40 μ m | 50 μ m | 50 μ m |
| Shear strenght (100x100 μ m pad) | 150 g | 50 g | 80 g |
| Wafer edge exclusion | 2-3 mm | n.a. | n.a. |
| Bump mask design/layout | PT wafer questionnaire, see www.pactech.de | GDS II data, step&repeat | GDS II data, step&repeat |

* depending on pad-pitch and pad design rules

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